IN THE CLAIMS:

Please cancel claims 89-105, 110-141, and 148-171 without prejudice as indicated below.

Please add claims 172-175 as indicated below.

Please amend claims 1, 18-21, 28-30, 41-43, 46, 106, 142, 145, and 146 as indicated below.

A listing of the status of all claims 1-171 in the present patent application is provided below.

1 (Currently Amended). An integrated circuit device for receiving a signal transmitted via an electrical signal conductor, the integrated circuit device comprising:

a first receiver circuit to sample the signal according to at least two threshold levels to generate data samples;

a level sampler to sample the signal to generate error samples; and

an adaptive module to adjust the at least two threshold levels according to the data samples from the first receiver circuit and the error samples from the level sampler;

the first receiver circuit including:

a first sampling circuit to sample the signal and generate a first sample value that indicates whether the signal exceeds a first threshold level;

_____a second sampling circuit to sample the signal and generate a second sample value that indicates whether the signal exceeds a second threshold level; and

_____a first select circuit coupled to receive the first and second sample values from the first and second sampling circuits and configured to select, according to a previously generated sample value, either the first sample value or the second sample value to be output as a selected sample value.

2 (Original). The integrated circuit device of claim 1 further comprising a first storage circuit to store the previously generated sample value, the first storage circuit having an output coupled to a select input of the first select circuit to output the previously generated sample value thereto.

3 (Original). The integrated circuit device of claim 2 wherein the first storage circuit has a data input coupled to the first select circuit to receive the selected sample value and a clock input to receive a first clock signal, the first storage circuit being configured to store the selected sample value in response to a transition of the first clock signal.

4 (Original). The integrated circuit device of claim 3 wherein

the selected sample value, when stored in the first storage circuit, constitutes the previously generated sample value in relation to a subsequent pair of sample values generated by the first and second sampling circuits.

5 (Original). The integrated circuit device of claim 1 wherein the previously generated sample value is generated by one of the first and second sampling circuits prior to generation of the first sample value and the second sample value.

6 (Original). The integrated circuit device of claim 1 further comprising:

a third sampling circuit to sample the signal and generate a third sample value that indicates whether the signal exceeds the first threshold level; and

a fourth sampling circuit to sample the signal and generate a fourth sample value that indicates whether the signal exceeds the second threshold level.

7 (Original). The integrated circuit device of claim 6 further comprising a second select circuit coupled to receive the third and fourth sample values from the third and fourth sampling circuits, the second select circuit being configured to select

either the third sample value or the fourth sample value to be stored in the first storage circuit as the previously generated sample value.

8 (Original). The integrated circuit device of claim 7 wherein the first and second sampling circuits are configured to sample the signal in response to a first clock signal, and wherein the third and fourth sampling circuits are configured to sample the signal in response to a second clock signal.

9 (Original). The integrated circuit device of claim 8 wherein the second clock signal is phase offset from the first clock signal by a portion of a cycle of the first clock signal such that the third and fourth sample values are generated at a different time than the first and second sample values.

10 (Original). The integrated circuit device of claim 9 wherein the second clock signal is phase offset by a half-cycle of the first clock signal.

11 (Original). The integrated circuit device of claim 1 wherein the first sampling circuit comprises a comparator circuit to compare the signal with a first threshold voltage to determine

whether the signal exceeds the first threshold level.

12 (Original). The integrated circuit device of claim 11 further comprising a threshold generating circuit to generate the first threshold voltage.

13 (Original). The integrated circuit device of claim 1 wherein the signal is a differential signal having a first signal component and a second signal component, the second signal component being a complement of the first signal component.

14 (Original). The integrated circuit device of claim 13 wherein the first sampling circuit comprises a differential comparator circuit to compare the differential signal against the first threshold level.

15 (Original). The integrated circuit device of claim 14 wherein the first threshold level exceeds the common mode of the differential signal.

16 (Original). The integrated circuit device of claim 15 wherein the common mode of the differential signal exceeds the second threshold level.

17 (Original). The integrated circuit device of claim 16 wherein the common mode of the differential signal is substantially centered between the first and second threshold levels.

18 (Currently Amended). The integrated circuit device of claim 14 wherein the first threshold level exceeds the common mode of the differential signal by a voltage that corresponds to a level of inter-symbol interference produced by at least one prior signal transmission on the electrical signal ~~transmission~~ conductor.

19 (Currently Amended). The integrated circuit device of claim 1 wherein the signal is a multi-level signal representative of more than a single binary bit, and wherein the first sample value generated by the first sampling circuit comprises more than one binary bit.

20 (Currently Amended). An ~~The~~ integrated circuit device ~~of claim 1 further~~ for receiving a signal transmitted via an electrical signal conductor, the integrated circuit device comprising:

a first sampling circuit to sample the signal and generate a first sample value that indicates whether the signal exceeds a first threshold level;

a second sampling circuit to sample the signal and generate a second sample value that indicates whether the signal exceeds a second threshold level;

a first select circuit coupled to receive the first and second sample values from the first and second sampling circuits and configured to select, according to a previously generated sample value, either the first sample value or the second sample value to be output as a selected sample value;

a third sampling circuit to compare the signal with a third threshold level and to generate error samples that indicate whether the signal exceeds or is below the third threshold level; and

a threshold generating circuit to adjust the third threshold level until the error samples indicate that the third threshold level substantially matches a first selected level of the signal.

21 (Currently Amended). The integrated circuit device of claim 20 further comprising a fourth comparator circuit to compare the signal with a fourth threshold level and to generate error

samples that indicate whether the signal exceeds or is below the ~~third~~ fourth threshold level, and wherein the threshold generating circuit is configured to adjust the fourth threshold level until the error samples indicate that the fourth threshold level substantially matches a second selected level of the signal.

22 (Original). The integrated circuit device of claim 21 wherein the threshold generating circuit is further configured to generate a first control signal based on the third and fourth threshold levels and to output the first control signal to the first sampling circuit to establish the first threshold level therein.

23 (Original). The integrated circuit device of claim 22 wherein the first control signal is a voltage at the first threshold level.

24 (Original). The integrated circuit device of claim 22 wherein the first control signal is a digital value representative of the first threshold level.

25 (Original). The integrated circuit device of claim 22

wherein the threshold generating circuit is configured to generate the first control signal based on an average of the third and fourth threshold levels.

26 (Original). The integrated circuit device of claim 22 wherein the threshold generating circuit is configured to generate the first control signal based on difference between the third and fourth threshold levels.

27 (Original). The integrated circuit device of claim 22 wherein the threshold generating circuit is further configured to generate a second control signal based on the third and fourth threshold levels, and to output the second control signal to the second sampling circuit to establish the second threshold level therein.

28 (Currently Amended). The integrated circuit device of claim 22 wherein the threshold generating circuit is further configured to generate a second control value based on the first control value and to output the second control value to the second sampling circuit to establish the second threshold level therein.

29 (Currently Amended). The integrated circuit device of claim 28 wherein the threshold generating circuit is configured to generate the second control value by complementing the first control value.

30 (Currently Amended). A method of operation within an integrated circuit device, the method comprising:

receiving a data signal from an external electrical signaling path;

generating a first data sample having one of at least two states according to whether the data signal exceeds a first threshold level;

generating a second data sample having one of the at least two states according to whether the data signal exceeds a second threshold level;

generating an error sample that indicates whether the data signal exceeds or is below a third threshold level, wherein the first, second, and third threshold levels are generated based at least in part upon the error sample; and

selecting either the first data sample or the second data sample to be a selected sample of the data signal.

31 (Original). The method of claim 30 wherein selecting either

the first data sample or the second data sample to be the selected sample comprises selecting either the first data sample or the second data sample according to whether a third data sample has a first state or a second state.

32 (Original). The method of claim 31 further comprising generating the third data sample prior to generating the first and second data samples.

33 (Original). The method of claim 30 wherein generating a first data sample comprises generating a first data sample having one of two binary states according to whether the data signal exceeds a first threshold.

34 (Original). The method of claim 30 wherein generating a first data sample comprises generating a first data sample having one of more than two possible states.

35 (Original). The method of claim 30 wherein the data signal is a differential signal and wherein the first threshold level is above a common mode of the data signal, and the second threshold level is below the common mode of the data signal.

36 (Original). The method of claim 35 wherein the common mode of the data signal is substantially centered between the first and second threshold levels.

37 (Original). The method of claim 30 further comprising:

determining a first voltage level of the data signal;

determining a second voltage level of the data signal; and

generating the first threshold level based on the first and second voltage levels of the data signal.

38 (Original). The method of claim 37 wherein generating the first threshold level based on the first and second voltage levels comprises averaging values representative of the first and second voltage levels to generate a first control value that corresponds to the first threshold level.

39 (Original). The method of claim 38 wherein the first control value is a voltage level.

40 (Original). The method of claim 38 wherein the first control value is a digital value.

41 (Currently Amended). A ~~The~~ method of ~~claim 37~~ operation

within an integrated circuit device, the method comprising:

receiving a data signal from an external electrical signaling path;

determining a first voltage level of the data signal;

determining a second voltage level of the data signal;

generating a first threshold level based on the first and second voltage levels of the data signal;

generating a first data sample having one of at least two states according to whether the data signal exceeds the first threshold level;

generating a second data sample having one of the at least two states according to whether the data signal exceeds a second threshold level; and

selecting either the first data sample or the second data sample to be a selected sample of the data signal;

wherein generating the first threshold level based on the first and second voltage levels comprises subtracting a value representative of the first voltage level from a value representative of the second voltage level to generate a first control value, the first control value corresponding to the first threshold level.

42 (Currently Amended). An integrated circuit device for

receiving a signal transmitted via an electrical signal conductor, the integrated circuit device comprising:

a first receive circuit clocked by a first clock signal and a second receive circuit clocked by a second clock signal, the second clock signal having a phase offset from the first clock signal, the first receive circuit including a first pair of sampling circuits and a first select circuit, the first pair of sampling circuits to capture a first pair of samples of the signal in response to ~~a~~ the first clock signal, the first select circuit to select one of the first pair of samples according to a first previously generated sample value output from the second receive circuit; and

a second receive circuit having a second pair of sampling circuits and a second select circuit, the second pair of sampling circuit to capture a second pair of samples of the signal in response to ~~a~~ the second clock signal~~; and~~

~~a first select circuit coupled to the first pair of sampling circuits and configured to select one sample of the first pair of samples according to a state of a selected sample of the second pair of samples~~.

43 (Currently Amended). The integrated circuit device of 42 ~~further comprising a second select circuit coupled to the second~~

~~pair of sampling circuits to select the selected sample of the second pair of samples~~ wherein the first clock signal and the second clock signal are offset by one-half of a clock cycle.

44 (Original). The integrated circuit device of claim 43 further comprising a first storage circuit coupled to receive the one sample of the first pair of samples from the first select circuit and configured to store the one sample of the first pair of samples in response to the first clock signal.

45 (Original). The integrated circuit device of claim 44 wherein an output of the first storage circuit is coupled to a select input of the second select circuit such that the state of a sample stored in the first storage circuit determines which sample of the second pair of samples is selected by the second select circuit.

46 (Currently Amended). An ~~The~~ integrated circuit device ~~of claim 44 further comprising~~ for receiving a signal transmitted via an electrical signal conductor, the integrated circuit device comprising:

a first pair of sampling circuits to capture a first pair of samples of the signal in response to a first clock signal;

a second pair of sampling circuits to capture a second pair of samples of the signal in response to a second clock signal;

a first select circuit coupled to the first pair of sampling circuits and configured to select one sample of the first pair of samples according to a state of a selected sample of the second pair of samples;

a second select circuit coupled to the second pair of sampling circuits and configured to select the selected sample of the second pair of samples;

a first storage circuit coupled to receive the one sample of the first pair of samples from the first select circuit and configured to store the one sample of the first pair of samples in response to the first clock signal; and

a second storage circuit coupled to receive the selected sample of the second pair of samples from the second select circuit and configured to store the selected sample of the second pair of samples in response to the second clock signal.

47 (Original). The integrated circuit device of claim 46 wherein an output of the second storage circuit is coupled to a select input of the first select circuit such that the state of a sample stored in the second storage circuit determines which sample of the first pair of samples is selected by the first

select circuit.

48 (Original). The integrated circuit device of claim 42 wherein the first clock signal is phase offset from the second clock signal by a portion of a cycle of the second clock signal such that the first pair samples are generated at a different time than the second pair of values.

49 (Original). The integrated circuit device of claim 42 wherein the signal is a differential signal and wherein each sampling circuit of the first pair of sampling circuits comprises a differential sampling circuit to generate a respective sample of the first pair of samples.

50 (Original). The integrated circuit device of claim 42 wherein a first sampling circuit of the first pair of sampling circuits is configured to determine whether the signal exceeds a first threshold level, and wherein a second sampling circuit of the first pair of sampling circuits is configured to determine whether the signal exceeds a second threshold level.

51 (Original). The integrated circuit device of claim 42 wherein the signal is a differential signal having a first

common mode level when at a steady state, and wherein the first common mode level is lower than the first threshold level and above the second threshold level.

52 (Original). The integrated circuit device of claim 51 wherein the first common mode level is substantially centered between the first and second threshold levels.

53 (Original). A dual mode receive circuit comprising:

compare circuitry to generate first and second samples of an input data signal, each sample having either a first state or a second state according to whether the input data signal exceeds a respective one of first and second threshold levels; and

decision circuitry to generate a received data value based on the first and second samples, the decision circuitry being operable in a first mode to generate a data value having a most significant bit according to the state of the first sample and a least significant bit based, at least in part, on the state of the second sample, the decision circuitry further being operable in a second mode to select either the first sample or the second sample to be the received data value.

54 (Original). The dual mode receive circuit of claim 53 wherein the compare circuitry is configured to generate a third sample according to whether the input data signal exceeds a third threshold level.

55 (Original). The dual mode receive circuit of claim 54 wherein, in the first mode, the decision circuitry is configured to generate the least significant bit of the data value according to the states of the second and third samples.

56 (Original). The dual mode receive circuit of claim 55 wherein the decision circuitry is configured to generate the least significant bit of the data value in either the first state or the second state according to whether the second and third samples have the same state or different states.

57 (Original). The dual mode receive circuit of claim 56 wherein the decision circuitry comprises an exclusive-OR logic circuit to generate the lest significant bit of the data value by exclusive-ORing the second and third samples.

58 (Original). The dual mode receive circuit of claim 53 wherein the compare circuitry is configured to generate the

first and second samples of the input data signal in response to a transition of a first clock signal.

59 (Original). The dual mode receive circuit of claim 53 further comprising a configuration control circuit to store a mode select value, the dual mode receive circuit being responsive to the mode select value to operate in either the first mode or the second mode.

60 (Original). The dual mode receive circuit of claim 53 further comprising a threshold generating circuit, the threshold generating circuit being configured to determine first and second signal levels of the input data signal and to generate the first and second threshold levels based on the first and second signal levels.

61 (Original). The dual mode receive circuit of claim 53 wherein, when the dual mode circuit is operated in the first mode, the first and second signal levels of the input signal are indicative of a signal swing of the input data signal, and wherein the threshold generating circuit is further configured to establish the first threshold level at a first voltage level substantially centered within the signal swing.

62 (Original). The dual mode receive circuit of claim 61 wherein the threshold generating circuit is further configured to establish the second threshold level at a second voltage level substantially centered between the first voltage level and a first peak level of the signal swing.

63 (Original). The dual mode receive circuit of claim 62 wherein the first peak level of the signal swing is an upper peak of the signal swing and wherein the threshold generating circuit is further configured to generate a third threshold level that is substantially centered between the first voltage level and a lower peak level of the signal swing.

64 (Original). The dual mode receive circuit of claim 53 wherein, in the second mode, the decision circuitry is operable to select either the first sample or second sample according to whether a third sample is in the first state or the second state, the third sample being generated prior to the first and second samples.

65 (Original). The dual mode receive circuit of claim 64 wherein the decision circuitry comprises a select circuit having

first and second inputs to receive the first and second samples, respectively, and a select input coupled to receive the third sample, the select circuit being configured to output either the first sample or the second sample as the received data value according to the state of the third sample.

66 (Original). The dual mode receive circuit of claim 65 further comprising a storage circuit coupled to receive the received data value from the select circuit, the received data value constituting the third sample in relation to subsequent instances of the first and second samples generated by the compare circuitry.

67 (Original). The dual mode receive circuit of claim 53 further comprising a threshold generating circuit, the threshold generating circuit being configured to generate the first and second thresholds at a first pair of voltage levels when the dual mode circuit is operated in the first mode, and to generate the first and second thresholds at a second pair of voltage levels when the dual mode circuit is operated in the second mode.

68 (Original). The dual mode receive circuit of claim 67

wherein the first pair of voltages are generated according to a signal swing of the input data signal.

69 (Original). The dual mode receive circuit of claim 68 wherein the threshold generating circuit comprises a level sampling circuit to determine the signal swing of the input data signal.

70 (Original). The dual mode receive circuit of claim 69 wherein the level sampling circuit is configured to determine a first voltage level of the input data signal that corresponds to a first symbol value, and a second voltage level of the input data signal that corresponds to a second symbol value, the signal swing of the input data signal being determined based on the first and second voltage levels.

71 (Original). The dual mode receive circuit of claim 68 wherein the second pair of voltages are generated according to a level of inter-symbol interference detected in the input data signal.

72 (Original). A method of operation within an integrated circuit device, the method comprising:

generating first and second samples of an input data signal, each sample having either a first state or a second state according to whether the input data signal exceeds a respective one of first and second threshold levels;

generating a first received data value based on the first and second data samples if a mode select signal is in a first state; and

generating a second received data value based on the first and second data samples if the mode select signal is in a second state, wherein the second received data value includes more constituent bits than the first received data value.

73 (Original). The method of claim 72 wherein the second received data value comprises at least two constituent bits.

74 (Original). The method of claim 73 wherein the first received data value comprises one bit.

75 (Original). The method of claim 72 wherein generating the second received data value comprises:

generating a most significant bit of the second received data value according to the state of the first sample; and

generating a least significant bit of the second received

data value based, at least in part, on the state of the second sample.

76 (Original). The method of claim 72 further comprising generating a third sample having either the first state or the second state according to whether the input data signal exceeds a third threshold level.

77 (Original). The method of claim 76 wherein generating the second received data value comprises:

generating a most significant bit of the second received data value according to the state of the first sample; and

generating a least significant bit of the second received data value according to the states of the second and third samples.

78 (Original). The method of claim 77 wherein generating the least significant bit comprises generating the least significant bit in either the first state or the second state according to whether the second and third samples have the same state or different states.

79 (Original). The method of claim 77 wherein generating the

least significant bit comprises generating an exclusive-OR combination of the second and third samples.

80 (Original). The method of claim 72 wherein generating first and second samples of an input data signal comprises sampling the input data signal in response to a transition of a first sample control signal.

81 (Original). The method of claim 80 wherein the first sample control signal is a clock signal.

82 (Original). The method of claim 72 wherein generating the first received data value comprises selecting either the first sample or the second sample to be the received data value.

83 (Original). The method of claim 82 wherein selecting either the first sample or the second sample to be the received data value comprises selecting either the first sample or the second sample according to whether a third sample is in the first state or the second state.

84 (Original). The method of claim 83 further comprising generating the third sample prior to generating the first and

second samples.

85 (Original). The method of claim 72 further comprising generating the first and second threshold levels.

86 (Original). The method of claim 85 wherein generating the first and second threshold levels comprises generating a first pair of threshold levels when the mode select signal is in the first state, and generating a second pair of threshold levels when the mode select signal is in the second state.

87 (Original). The method of claim 86 wherein generating the first pair of threshold levels comprises generating the first pair of threshold levels based on a signal swing of the input signal.

88 (Original). The method of claim 86 wherein generating the second pair of threshold levels comprises generating the second pair of threshold levels based on a level of inter-symbol interference in the input data signal.

89-105 (Cancelled).

106 (Currently Amended). An integrated circuit device comprising:

a first sampling circuit to sample an input data signal at a time that corresponds to a transition interval within the input data signal, the first sampling circuit being configured to generate a sample value having either a first state or a second state according to whether the input data signal, when sampled, is above or below a selected threshold level; and

a threshold generating circuit to establish the selected threshold level ~~within the first sampling circuit~~, the threshold generating circuit establishing the selected threshold level at a first threshold level if a mode select signal is in a first state, and establishing the selected threshold level at a second threshold level if the mode select signal is in a second state.

107 (Original). The integrated circuit device of claim 106 wherein the first state of the mode select signal corresponds to a binary signal reception mode within the integrated circuit device, and wherein the second state of the mode select signal corresponds to a multi-level signal reception mode within the integrated circuit device.

108 (Original). The integrated circuit device of claim 106

further comprising a clock recovery circuit to generate a first clock signal that transitions at the time that corresponds to the transition interval within the input data signal.

109 (Original). The integrated circuit device of claim 108 wherein the clock recovery circuit is coupled to receive the sample value generated by the first sampling circuit and is configured to advance or retard the phase of the first clock signal based, at least in part, on the state of the sample value.

110-141 (Cancelled).

142 (Currently Amended). A method of operation within a signaling system, the method comprising:

outputting a sequence of data values onto an electrical signal conductor during successive transmission intervals, the sequence of data values forming a data signal on the electrical signal conductor;

generating, during ~~each of a sequence of data reception intervals~~ a first data reception interval, a first data sample having either a first state or second state according to whether a signal level of the electrical signal conductor exceeds a

first threshold level and a second data sample having either the first state or second state according to whether the signal level exceeds a second threshold level;

generating, during the first data reception interval, an error sample that indicates whether the signal level of the electrical signal conductor exceeds or is below a third threshold level;

outputting, during a second data reception interval after the first data reception interval, a selected data sample, the selected data sample being selected from the first data sample and the second data sample according a data sample generated during a third data interval prior to the second data reception interval; and

~~selecting, during each of the data reception intervals after a first one of the data reception intervals, either the first data sample or the second data sample to be a received data value according to the state of at least one received data value selected during a prior reception interval~~

outputting the error sample during the second data reception interval.

143 (Original). The method of claim 142 wherein selecting either the first data sample or the second data sample to be the

received data value comprises selecting either the first data sample or the second data sample to be the received data value according to the state of a received data value selected during an immediately preceding one of the reception intervals.

144 (Original). The method of claim 142 wherein selecting either the first data sample or the second data sample to be the received data value according to the state of the at least one received data value comprises selecting, during one of the data reception intervals, either the first data sample or the second data sample to be the received data value according to the state of N received data values selected during N respective reception intervals that precede the one of the data reception intervals, N being an integer value greater than zero.

145 (Currently Amended). The method of claim 144 wherein outputting the sequence of data values comprises outputting an equalizing signal onto the electrical signal conductor during each one of the transmission intervals to reduce inter-symbol interference resulting from data values transmitted more than N transmission intervals prior to the one of the transmission intervals.

146 (Currently Amended). The method of claim 145 wherein outputting an equalizing signal onto the electrical signal conductor comprises generating an equalizing signal according to at least one of the data values transmitted more than N transmission intervals prior to the one of the transmission intervals.

147 (Original). The method of claim 146 wherein generating the equalizing signal further comprises generating the equalization signal in an output driver in accordance with a weighting value that controls a signal drive strength of the output driver.

148-171 (Cancelled).

172 (New). The integrated circuit device of claim 1, wherein the first receiver circuit outputs in parallel two successive data samples to the adaptive module.

173 (New). The integrated circuit device of claim 172, wherein the level sampler includes storage circuits to buffer the error samples before the error samples are provided to the adaptive module.

174 (New). The integrated circuit device of claim 1, further comprising a second receiver circuit to sample the signal according to the at least two threshold levels to generate data samples, the second receiver circuit outputting the previously generated sample value to the first receiver circuit.

175 (New). An integrated circuit device for receiving signals transmitted in parallel via a data bus, the integrated circuit device comprising:

a plurality of receive circuits to receive respective ones of the signals via respective signal lines of the data bus, the plurality of receive circuits including a first receive circuit to receive a first one of the signals from a first signal line of the data bus;

a level sampler to sample the first one of the signals to generate at least one error sample; and

an adaptive module to produce at least one pair of threshold values according to outputs from the first receive circuits and the level sampler, and to provide the at least one pair of threshold values to the plurality of receive circuits, wherein a respective receive circuit includes at least one pair of samplers to produce at least one pair of sample values of a respective signal by comparing a signal level of the respective

signal with the at least one pair of threshold values, and wherein the respective receive circuit further includes selection circuitry to select one of the sample values according to a previously produced sample value.